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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/478,122

01/05/2000

Laurence A. Thompson

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1276

7590

08/22/2005

PERKINS COLE LLP
101 JEFFERSON DRIVE
MENLO PARK, CA 94025-1114

EXAMINER

LAO, LUN S

ART UNIT

PAPER NUMBER

2644

DATE MAILED: 08/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/478,122	THOMPSON, LAURENCE A.	
	Examiner	Art Unit	
	Lun-See Lao	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 October 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 36-49 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 36-49 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Introduction

1. The request filed on 10-24-2004 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/478,122 is acceptable and a CPA has been established. An action on the CPA follows.

2. This action is response to amendment filed on 10-24-2004. Claims 1-35 have been cancelled and Claims 36-49 have been added.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 36-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (US PAT. 6,272,153).

Consider claim 36, Huang teaches that an apparatus for delaying an audio signal comprising:

a first register (see fig.5, (504, input buffer) receptive to a digital audio signal;
an audio format detection (510, 512) coupled to the first register (504) and operative to detect a format of the digital audio signal;

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a memory controller (508,518) coupled to the FIFO register (output buffer and see col. 7 line 30-col.8 line 43 and col.9 line 15-23);

a memory chip (522, 524) coupled to the memory controller(508, 518);

a write address generator (502) coupled to the audio format detection (510,512) and memory controller (508, 518);

a read address generator (502) coupled to the memory controller (508, 518 and see col. 7 line 30-col. 8 line 43); and

a second FIFO register (542, out put buffer) coupled to the memory controller (508, 518) and operative to provide a time delay in the digital audio signal the duration of which is related to the detected format of the digital audio signal (see col.8 line 30-col. 9 line 40), but Huang does not clearly teach first FIFO register, however, Huang does indicate FIFO output buffer (see col.9 line 15-23) and FIFO register is well known in the art.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Huang by implementing a particular audio decoder architecture as claim for the purpose of acquiring the desired audio signal running faster.

Consider claims 37-39, Huang teaches that the apparatus of the digital audio signal further comprises a serial audio clock signal and a plurality of accompanying signals (see col. 8 line 30-col.9 line 40); and the apparatus of the accompanying signals further comprises a data signal and a frame synchronization signal (see col. 7 line 30-col.8 line 12); and the apparatus of the audio format detection (see fig. 5(508,512) is operable to

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detect a number of edge (by state machines) transitions in the serial audio clock signal and provide a corresponding detected count (see col. 7 line 30-col. 9 line 23).

5. Claims 40-44 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al (US PAT. 6,272,153) in view of Kuwaoka (US PAT. 6,449,519).

Consider claim 40, Huang teaches that the apparatus of the audio format detection (see fig.5, 510, 512) further comprises a plurality of model data, wherein each model data represents one of a plurality of audio signal formats (see col. 7 line 30-col. 8 line 43), but Huang does not clearly teach a corresponding one of a plurality of time delay data, wherein the detected count is compared to the model data, the audio format detection operable to provide the delay data representing the model data that is equal to the detected count.

However, Kuwaoka teaches a corresponding one of a plurality of time delay data, wherein the detected count (28,25i) is compared (23,24) to the model data, the audio format (formation) detection (25i, 28) operable to provide the delay data representing the model data that is equal to the detected count (see col.8 line 28-col.9 line 50).

Therefore, it would obvious to one of ordinary skill in the art at the time invention was made to combine the teaching of Kuwaoka into Huang to provide a compact and high-performance audio information processing apparatus.

Consider claims 41-42, Huang teaches that the apparatus of the processed clock signal is synchronized to a reference clock (see col.6 line 40-col. 7 line 65 and col. 13-col.9 line 41); and the apparatus of the audio format detection (see fig.5, 510, 512) is

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operable to provide a processed clock signal by dividing (by state machine) the serial clock signal by a constant (see col.6 line 40-col. 7 line 65 and col. 13-col.9 line 41).

Consider claims 43-44, Kuwaoka teaches the apparatus of the processing device is operable to compare a new time delay data (current audio data) to an old time delay data (audio data of a before), the processing device operable to reconfigure a buffer if the new time delay data is not equal to the old time delay data (see col.9 line 17-35); and the apparatus of the detected count is compared to the model data by a plurality of comparators (see fig.3, (23,24) and col.9 line 17-57).

Consider claim 47, Kuwaoka teaches that the apparatus of the processing device further comprises a memory unit (see fig.3, 25) to provide the time delay corresponding to the time delay data (see col.8 lines 27-65).

6. Claims 45-46 and 48-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al (US PAT. 6,272,153) as modified by Kuwaoka (US PAT. 6,449,519) as applied to claims 40-44 above, and further in view of Sueyoshi et al (US PAT. 6,233,562).

Consider claim 45, Huang and Kuwaoka do not teach the apparatus of the provided time delay data is a first offset value, the processing device operable to resize a write address pointer with the offset value.

However Sueyoshi teaches the apparatus of the provided time delay data is a first offset value (see fig.1 4a, sent by pointer controller), the processing device operable to

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resize a write address pointer (actual pointer and temporary pointer) with the offset value (sent by pointer controller, 4a and see col.4 lines 2-42);

Therefore, it would obvious to one of ordinary skill in the art at the time invention was made to combine the teaching of Sueyoshi in to the teaching of Huang and Kuwaoka for reducing the required capacity of the buffer memory provided there between while synchronizing the audio signal out from the internal decoder and the audio signal output from the external decoder.

Consider claim 46 Sueyoshi teaches the apparatus of the provided time delay data is a second offset value (sent by pointer controller, 4a), the processing device operable to resize a read address pointer (actual pointer and temporary pointer) with the offset value (sent by pointer controller, 4a and see col.4 lines 2-42).

Consider claims 48-49, Sueyoshi teaches apparatus of the processing device (see fig.1, 2) further comprises a first parameter (write = replace information) and a second parameter (read information), the first parameter configured according to the provided time delay data (see col.4 lines 2-44); and the apparatus of the first parameter (information) is a write address parameter (actual pointer and temporary pointer), the second parameter (information) is a read address parameter (actual pointer and temporary pointer), and the memory unit is a buffer (see col.4 lines 2-44).

Response to Arguments

7. Applicant's arguments with respect to claims 36-49 have been considered but are moot in view of the new ground(s) of rejection.

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Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Rao (US PAT. 6,205,223) is recited to show other related the audio signal delay apparatus and method.

9. Any response to this action should be mailed to:

Mail Stop ____ (explanation, e.g., Amendment or After-final, etc.)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Facsimile responses should be faxed to:
(703) 872-9306

Hand-delivered responses should be brought to:
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lao,Lun-See whose telephone number is (571) 272-7501. The examiner can normally be reached on Monday-Friday from 8:00 to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chin Vivian, can be reached on (571) 272-7848.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 whose telephone number is (571) 272-2600.

Lao,Lun-See
Patent Examiner
US Patent and Trademark Office
Knox
571-272-7501

Date 08-10-2005


VIVIAN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

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